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EXAMINER	
SUCH, MATTHEW W	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

REPLACEMENT **Office Action Summary**	**Application No.** 10/607,769	**Applicant(s)** HARELAND ET AL.	
	Examiner Matthew W. Such	**Art Unit** 2891	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 August 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Replacement Office Action

1. The Examiner notes that the present Office Action serves as a replacement for the Office Action mailed 14 August 2007 since an amendment was submitted by Applicant on 6 August 2007 and the amendment has not been examined on the merits.

As such, the statutory time period for response has been restarted.

Claim Objections

2. Claims 1 and 7 is objected to because of the following informalities:

a. The phrase "portion said bottom surface" in Line 5 of Claim 1 should read "portion of said bottom surface". Appropriate correction is required.

b. The phrase "opposite a bottom, said" in Line 2 of Claim 7 should read "opposite a bottom surface, said". Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claim 7 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 7 recites the limitation "said insulating substrate" in Line 3. There is insufficient antecedent basis for this limitation in the claim. For the purposes of compact prosecution, the Examiner provisionally interprets the phrase to be "an insulating substrate". Claim 7 also recites the limitation "said silicon body" in Line 16. There is insufficient antecedent basis for this limitation in the claim. For the purposes of compact prosecution, the Examiner provisionally interprets the phrase to be "said semiconductor body". The Examiner further notes that treating the limitation as a silicon body would render claim 9 indefinite because the semiconductor body cannot be two different materials at the same time (i.e. silicon and silicon-germanium or silicon and gallium arsenide).

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1 and 7 are rejected under 35 U.S.C. 102(b) as being anticipated by Gotou ('999).

a. Regarding claim 1, Gotou teaches a non-planar semiconductor device with a semiconductor body (Element 33; Figs 8A-8C, 9A-9C) having a top surface and a bottom surface formed above an insulating substrate (Elements 31 and 32), wherein the semiconductor body has a pair of laterally opposite sidewalls (left and right side of Element 33 in Figs. 8B and 9B, for example). A gate dielectric (Element 37) is formed on the top surface, bottom surface, and on laterally opposite sidewalls of the semiconductor body. A gate electrode (Element 38; Figs 8A-8C, 9A-9C, for example) is formed on the top surface of the semiconductor body, adjacent to the gate dielectric on the laterally opposite sidewalls of the semiconductor body, and beneath the bottom surface of the semiconductive body. The gate electrode has a pair of laterally opposite sidewalls oriented perpendicularly to the laterally opposite sidewalls of the semiconductor body (see sidewalls formed at the interface between Elements 32 and 36 directly under Element 33 as depicted in Figs. 8C and 9C, for example). The gate electrode has a top portion and a bottom portion, wherein the bottom portion laterally undercuts the top portion at least on the laterally opposite sidewalls of the gate electrode (see sidewalls formed at the interface between Element 32 and 36 directly under Element 33 as depicted in Figs. 8C and 9C, for example). A pair of source/drain regions are formed in the semiconductor body (Elements 39 and 40, for example).

b. In so far as claim 7 is definite, Gotou teaches a non-planar semiconductor device comprising a semiconductor body (Element 33; Figs 8A-8C, 9A-9C) having a top surface opposite a bottom surface with laterally opposite sidewalls formed above an insulating

substrate of (Elements 31 and 32). A gate dielectric (Element 37) is formed on the top surface, laterally opposite sidewalls and on at least a portion of the bottom surface of the semiconductor body. A gate electrode (Element 38; Figs 8A-8C, 9A-9C, for example) is formed on the gate dielectric on the top surface of the semiconductor body, adjacent to the laterally opposite sidewalls of the semiconductor body, and beneath the bottom surface of the semiconductor body. The gate electrode has a pair of laterally opposite sidewalls oriented perpendicularly to the laterally opposite sidewalls of the semiconductor body (see sidewalls formed at the interface between Elements 32 and 36 as shown with the vertical gray lines added to Figs. 8C and 9C):

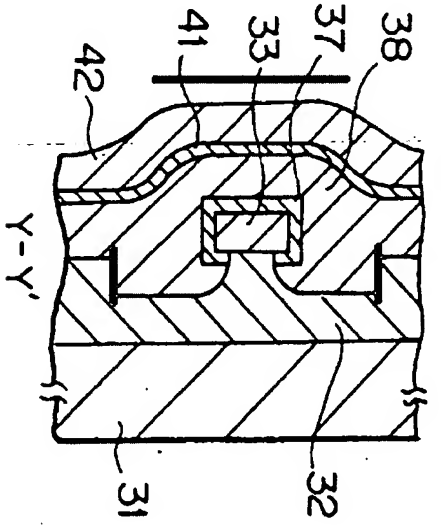

Fig. 9C

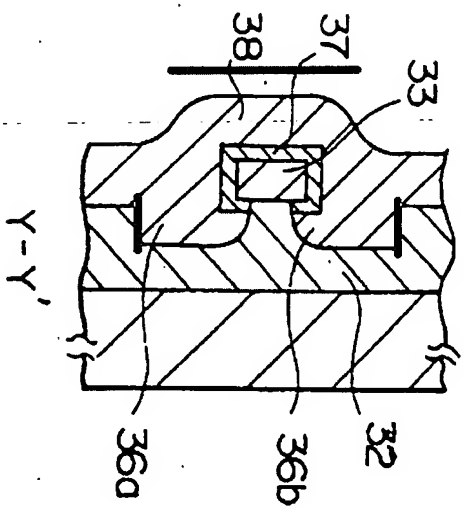

Fig. 8C

The gate electrode has a top portion above the insulating substrate and a bottom portion formed in the insulating substrate (see Figs. 8C and 9C, for example, with the bottom portion of Element 38 formed within Element 32). The bottom portion of the gate electrode has a larger width than the top portion of the gate electrode wherein the width is the dimension of the gate electrode that is oriented perpendicularly to the laterally opposite sidewalls of the semiconductor body (see the width between the vertical gray

lines is larger than the width of the horizontal gray line in Figs. 8C and 9C, for example). A pair of source/drain regions are formed in the semiconductor body on opposite sides of the gate electrode (Elements 39 and 40, for example).

7. Claims 1-5 are rejected under 35 U.S.C. 102(e) as being anticipated by Kim (`031).

a. Regarding claim 1, Kim teaches a non-planar semiconductor device with a semiconductor body (Elements 30 and 40) having a top surface and a bottom surface formed above an insulating substrate (Elements 10 and 20), wherein the semiconductor body has a pair of laterally opposite sidewalls (left and right side of Fig. 6B or 8C, for example; on of two different pairs can be chosen as the laterally opposite sidewalls). A gate dielectric (Elements 22 and 24) is formed on the top surface, bottom surface, and on laterally opposite sidewalls of the semiconductor body. A gate electrode (Element 80 in Fig. 6C or Element 90 in Fig. 8B, for example) is formed on the top surface of the semiconductor body, adjacent to the gate dielectric on the laterally opposite sidewalls of the semiconductor body, and beneath the bottom surface of the semiconductive body. The gate electrode has a pair of laterally opposite sidewalls oriented perpendicularly to the laterally opposite sidewalls of the semiconductor body (see relationship depicted in Figs. 6B to 6C and Figs. 8B to 8C, for example). The gate electrode has a top portion and a bottom portion, wherein the bottom portion laterally undercuts the top portion at least on the laterally opposite sidewalls of the gate electrode (see portion of Element 90 below Element 40 with sidewalls formed adjacent to Element 30 undercutting the portion

of Element 90 above Element 40 in Fig. 8B; see portion of Element 80 below Element 40 with sidewalls formed adjacent to Element 60 undercutting the portion of Element 80 above Element 40 in Fig. 6C, for example). A pair of source/drain regions are formed in the semiconductor body (Para. 0032 and 0035, for example).

b. Regarding claim 2, Kim teaches that the semiconductor body can be a single crystal silicon film (Element 40).

c. Regarding claim 3, Kim teaches that the semiconductor body can be silicon germanium (Element 30).

d. Regarding claim 4, Kim teaches that the gate electrode can be polysilicon, tungsten, tantalum, and metal nitrides (Para. 0038).

e. Regarding claim 5, Kim further teaches that insulating substrate comprises an oxide film (Element 20) on a monocrystalline silicon substrate (Element 10).

8. In so far as definite, claims 7-8 and 10-11 are rejected under 35 U.S.C. 102(e) as being anticipated by Song (`282).

a. Regarding claim 7, Song teaches a non-planar semiconductor device comprising a semiconductor body (Element 30; Fig. 8A-8C, 9A-9C) having a top surface opposite a

bottom surface with laterally opposite sidewalls formed above an insulating substrate of (Elements 10 and 20`; Figs. 8A-8C, 9A-9C). A gate dielectric (Elements 42 and 45; Figs. 8A-8C, 9A-9C) is formed on the top surface, laterally opposite sidewalls and on at least a portion of the bottom surface of the semiconductor body. A gate electrode (Element 62; Figs. 8A-8C, 9A-9C) is formed on the gate dielectric on the top surface of the semiconductor body, adjacent to the laterally opposite sidewalls of the semiconductor body, and beneath the bottom surface of the semiconductor body (Figs. 8C and 9C, for example). The gate electrode has a pair of laterally opposite sidewalls oriented perpendicularly to the laterally opposite sidewalls of the semiconductor body (Figs. 8A and 9A show the top view of the perpendicular orientation; Figs. 8B and 9B, for example, have the sidewalls of the semiconductor body in a plane parallel to the page and the sidewalls of the gate electrode running in a plane perpendicular to the plane of the page). The gate electrode has a top portion above the insulating substrate (see Figs. 8B and 9B, for example, with the top portion of Element 62 above Element 20`) and a bottom portion formed in the insulating substrate (see Figs. 8B and 9B, for example, with the bottom portion of Element 62 formed within Element 20`). The bottom portion of the gate electrode has a larger width than the top portion of the gate electrode wherein the width is the dimension of the gate electrode that is oriented perpendicularly to the laterally opposite sidewalls of the semiconductor body (see Figs. 8A-8B, 9A-9B). A pair of source/drain regions are formed in the semiconductor body on opposite sides of the gate electrode (Para. 0026-0028, for example).

b. Regarding claim 8, Song teaches that the semiconductor body is a single crystalline silicon film (Para. 0015).

c. Regarding claim 10, Song teaches that the gate electrode comprises, for example, silicon, tantalum, titanium, or metal nitrides thereof (Para. 0024).

d. Regarding claim 11, Song teaches that the insulating substrate comprises an oxide film (Elements 2 and 5) on a monocrystalline silicon substrate (Element 1).

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 3 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gotou (`999) in view of Yu (`869).

Gotou teaches the device of claims 1 and 7 wherein the semiconductor body material is silicon, but does not teach other conventional alternative materials.

Yu teaches using silicon-germanium as an alternative conventional semiconductor body material (Abstract; Col. 3, Lines 1-20) for devices formed on SOI substrates. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a silicon-

germanium channel material as taught by Yu in the device of Gotou. Yu teaches that germanium inclusion with silicon to produce a silicon-germanium material increases the charge carrier mobility of the channel region in a semiconductor body, thereby producing a faster device (Abstract; Col. 2, Lines 22-31; Col. 4, Lines 65-67).

11. Claims 4 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gotou (`999) in view of Kim (`031).

Gotou teaches the device of claims 1 and 7, but does not teach the conventional materials used for gate electrodes in gate-all-around devices.

Kim teaches that the gate electrode can be polysilicon, tungsten, tantalum, and metal nitrides (Para. 0038). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use any of the material taught by Kim as the all-around gate electrode of Gotou since Kim teaches that these materials have superior gap-filling capability when formed as all-around gate electrodes (Kim Para. 0038).

12. Claims 6 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gotou (`99) in view of Miyamoto (`914).

Gotou only teaches a single semiconductor body as a channel region of a transistor device and does not teach an additional semiconductor body with a top surface, a bottom surface, and a pair of laterally opposite sidewalls with a gate dielectric and gate electrode formed on each.

Miyamoto teaches using additional semiconductor bodies (Elements 6a-6d, for example) as channel regions each with a top surface, a bottom surface, and a pair of laterally opposite

sidewalls. A gate dielectric (Element 7) is formed on the top surface, bottom surface, and pair of laterally opposite sidewalls of the additional semiconductor bodies. A gate electrode (Element 8) is formed on the gate dielectric on the top surface, bottom surface, and the pair of laterally opposite sidewalls of the additional semiconductor bodies. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use an at one additional semiconductor body completely surrounded by gate dielectric and gate electrode as taught by Miyamoto in the device of Gotou. Miyamoto teaches that the inclusion of additional semiconductor bodies in a transistor increases the overall channel area and current capacity of the device thereby improving the quality of the device (Miyamoto Abstract, for example).

13. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kim (`031) in view of Miyamoto (`914).

Kim only teaches a single semiconductor body as a channel region of a transistor device in the configuration of claim 1 and does not teach an additional semiconductor body with a top surface, a bottom surface, and a pair of laterally opposite sidewalls with a gate dielectric and gate electrode formed on each.

Miyamoto teaches using additional semiconductor bodies (Elements 6a-6d, for example) as channel regions each with a top surface, a bottom surface, and a pair of laterally opposite sidewalls. A gate dielectric (Element 7) is formed on the top surface, bottom surface, and pair of laterally opposite sidewalls of the additional semiconductor bodies. A gate electrode (Element 8) is formed on the gate dielectric on the top surface, bottom surface, and the pair of laterally opposite sidewalls of the additional semiconductor bodies. It would have been obvious to one of

ordinary skill in the art at the time the invention was made to use an at one additional semiconductor body completely surrounded by gate dielectric and gate electrode as taught by Miyamoto in the device of Song. Miyamoto teaches that the inclusion of additional semiconductor bodies in a transistor increases the overall channel area and current capacity of the device thereby improving the quality of the device (Miyamoto Abstract, for example).

14. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Song (`282) in view of Yu (`869).

Song teaches the device of claim 7 wherein the semiconductor body material is single crystal silicon, but does not teach other conventional alternative materials.

Yu teaches using silicon-germanium as an alternative conventional semiconductor body material (Abstract; Col. 3, Lines 1-20) for devices formed on SOI substrates. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a silicon-germanium channel material as taught by Yu in the device of Song. Yu teaches that germanium inclusion with silicon to produce a silicon-germanium material increases the charge carrier mobility of the channel region in a semiconductor body, thereby producing a faster device (Abstract; Col. 2, Lines 22-31; Col. 4, Lines 65-67).

15. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Song (`282) in view of Miyamoto (`914).

Song only teaches a single semiconductor body as a channel region of a transistor device and does not teach an additional semiconductor body with a top surface, a bottom surface, and a pair of laterally opposite sidewalls with a gate dielectric and gate electrode formed on each.

Miyamoto teaches using additional semiconductor bodies (Elements 6a-6d, for example) as channel regions each with a top surface, a bottom surface, and a pair of laterally opposite sidewalls. A gate dielectric (Element 7) is formed on the top surface, bottom surface, and pair of laterally opposite sidewalls of the additional semiconductor bodies. A gate electrode (Element 8) is formed on the gate dielectric on the top surface, bottom surface, and the pair of laterally opposite sidewalls of the additional semiconductor bodies. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use an at one additional semiconductor body completely surrounded by gate dielectric and gate electrode as taught by Miyamoto in the device of Song. Miyamoto teaches that the inclusion of additional semiconductor bodies in a transistor increases the overall channel area and current capacity of the device thereby improving the quality of the device (Miyamoto Abstract, for example).

Claim Rejections - 35 USC § 102 / 35 USC § 103

16. Claims 2, 5, 8 and 11 are rejected under 35 U.S.C. 102(b) as anticipated by Gotou (`999) or, in the alternative, under 35 U.S.C. 103(a) as obvious over Gotou (`999).

Gotou teaches that the semiconductor body is formed from silion-on-insulator (SOI), single crystal silicon (Element 33) and that the insulating substrate comprises an oxide (Element 32) on a monocrystalline silicon substrate (Element 31). However, assuming *arguendo* that one were to interpret the reference of Gotou so narrowly such that SOI is not a single crystal silicon

channel and monocrystalline silicon substrate, it nevertheless would have been obvious to one of ordinary skill in the art at the time the invention was made to use single crystal silicon in order to provide a smooth, conventional, and inexpensive substrate as a seed for epitaxial growth of a single crystal silicon SOI layer in order to provide a defect free channel region for improved transistor device performance as well as increased integration with other devices, as is conventional.

Response to Arguments

17. Applicant's arguments with respect to claims 1-12 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

18. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

i. Skotnicki (`403), Yang (`324), Coronel (`968) and Rhee (`877) each teach various configurations for all-around gate electrodes for transistors;

ii. Bohr (`238) and Myrick (`885) each teach conventional SOI substrates.

Contact Information

19. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew W. Such whose telephone number is (571) 272-8895. The examiner can normally be reached on Monday - Friday 9AM-5PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bradley W. Baumeister can be reached on (571) 272-1722. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Matthew W. Such
Examiner
Art Unit 2891

MWS
12/22/07

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